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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/673,542
Filing Date: September 30, 2003
Appellant(s): LEE ET AL.

Wonjoo Suh
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed October 14th 2009 appealing from the Office action mailed June 17th 2009.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US 7196701 B2 Tsutsui 3-2007

The Applicant's Admitted Prior Art

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 18, 20, 22, 27 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (AAPA) and Tsutsui (US 7,196,701).

Regarding **Claim 5**, the AAPA teach a method for supplying power to a liquid crystal display comprising steps of:

taking a power source voltage having a constant level greater than 2.9V from a power source of a system (AAPA, Fig. 2); and

supplying the power source voltage greater than 2.9V to an interface circuit, a timing controller, and a data driving circuit, and a gate driving circuit for processing digital signal (AAPA, Fig. 2 VCC elements 11-14); and

raising or reducing the power source voltage greater than 2.9V using a DC-DC converter to generate a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH, and a gate low voltage VGL (AAPA, Fig. 2 element 16), wherein the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 are supplied to the data driving circuit (AAPA, Fig. 2

element 13), and the gate high voltage VGH and the gate low voltage VGL are supplied to the gate driving circuit (AAPA, Fig. 2 element 14).

The AAPA fails to teach that the power source is less than 2.9V. Tsutsui does, however, teach a similar power source, while in the power saving mode a *constant* low level voltage is provided without variation, used for the same function that is less than 3.1V (Tsutsui, Fig. 3 element 300 and power save control signal). A person of ordinary skill in the art upon analyzing Tsutsui would have reasonably used any voltage values that are appropriate for different loads, including voltages less than 2.9V. The exact voltage values used are dependent on the voltage that is required to drive the load and are completely arbitrary, and therefore it would have been obvious to try voltages less than 2.9V along with low power loads to achieve the predictable result of power conservation. Additionally, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the power saving power supply of Tsutsui in place of the generic power supply of the AAPA in order to reduce power consumption.

Regarding **Claim 18**, the AAPA teaches an apparatus for supplying power to a liquid crystal display comprising steps of:

a power source of a system for generating a power voltage having a constant level over 2.9V (AAPA, Fig. 2); and

an interface circuit, a timing controller, a data driving circuit, and a gate driving circuit for processing digital signal by taking the power source voltage (AAPA, Fig. 2 elements 11-14); and

a DC-DC converter for raising or reducing the power source voltage over 2.9V using a DC-DC converter to generate a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH, and a gate low voltage VGL (AAPA, Fig. 2 element 16), wherein the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 are supplied to the data driving circuit (AAPA, Fig. 2 element 13), and the gate high voltage VGH and the gate low voltage VGL are supplied to the gate driving circuit (AAPA, Fig. 2 element 14),

wherein the power source voltage is supplied to the interface circuit, the timing controller, the data driving circuit and the gate driving circuit.

The AAPA fails to teach that the power source is less than 2.9V. Tsutsui does, however, teaches a similar power source, while in the power saving mode a *constant* low level voltage is provided without variation, used for the same function that is less than 3.1V (Tsutsui, Fig. 3 element 300 and power save control signal). A person of ordinary skill in the art upon analyzing Tsutsui would have reasonably used any voltage values that are appropriate for different loads, including voltages less than 2.9V. The exact voltage values used are dependent on the voltage that is required to drive the load and are completely arbitrary, and therefore it would have been obvious to try voltages less than 2.9V along with low power loads to achieve the predictable result of power conservation. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the power saving power supply of Tsutsui in place of the generic power supply of the AAPA in order to reduce power consumption.

Regarding **Claim 20**, the AAPA further teaches:

the interface circuit receives a synchronous signal, a clock signal and digital video data from the system (AAPA, Fig. 2 element 11);

the timing controller controls the data driving circuit and the gate driving circuit by using the synchronous signal and the clock signal from the interface circuit (AAPA, Fig. 2 element 12),

wherein the data driving circuit supplies the digital video data to the liquid crystal panel and the gate driving circuit supplies a scan pulse to the liquid crystal panel (AAPA Fig. 2 elements 13-15).

Regarding **Claim 22**, the AAPA teaches a method for supplying a power to a liquid crystal display, having an interface circuit, a timing controller, a data driving circuit and a gate driving circuit for processing digital signal, (AAPA, Figs. 2 and 4) comprising the steps of:

providing a first power source voltage from a power source of a system wherein the first power source voltage is 3.3V (AAPA, Figs. 2 and 4 VCC);

supplying the first power source voltage having a constant level of 3.3V to the interface circuit, the timing controller, the data driving circuit and the gate driving circuit for processing digital signal of the interface circuit, the timing controller, the data driving circuit, and the gate driving circuit (AAPA, Figs. 2 and 4 VCC elements 11-14);

generating a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH, and a gate low voltage VGL from the first power source voltage of 3.3V using a DC-DC converter, (AAPA, Fig. 2 element 16),

supplying the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 are supplied to the data driving circuit (AAPA, Fig. 2 element 13), and the gate high voltage VGH and the gate low voltage VGL are supplied to the gate driving circuit (AAPA, Fig. 2 element 14).

The AAPA fails to teach a second power source voltage as claimed. Tsutsui does, however, teach a second power source voltage having a constant voltage level of less than 2.9V generated from the first power source voltage using a reducing circuit, the second power source voltage being used to process digital signal of the digital circuit devices and lower than the first power source voltage, and supplying the second power source voltage to the digital circuit devices (Tsutsui Figs. 2 and 7 VDD2 is supplied as driving circuitry). A person of ordinary skill in the art upon analyzing Tsutsui would have reasonably used any voltage values that are appropriate for different loads, including voltages less than 2.9V. The exact voltage values used are dependent on the voltage that is required to drive the load and are completely arbitrary, and therefore it would have been obvious to try voltages less than 2.9V along with low power loads to achieve the predictable result of power conservation. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the power saving power supply of Tsutsui in place of the generic power supply of the AAPA in order to reduce power consumption.

Regarding **Claim 27**, the AAPA teaches a method for supplying a power to a liquid crystal display, having digital circuit devices including an interface circuit, a timing

controller, a data driving circuit, and a gate driving circuit for processing digital signal, (AAPA, Fig. 2) comprising the steps of:

providing a power source voltage from a power source of a system wherein the first power source voltage has a constant level of 3.3V (AAPA, Figs. 2 and 4);

supplying the power source voltage to the interface circuit, the timing controller, the data driving circuit and the gate driving circuit (AAPA, Figs. 2 and 4 VCC elements 11-14);

generating a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH, and a gate low voltage VGL from the first power source voltage of 3.3V using a DC-DC converter, (AAPA, Fig. 2 element 16),

supplying the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 are supplied to the data driving circuit (AAPA, Fig. 2 element 13), and the gate high voltage VGH and the gate low voltage VGL are supplied to the gate driving circuit (AAPA, Fig. 2 element 14).

The AAPA fails to teach that the power source is less than 2.9V. Tsutsui does, however, teach a similar power source, while in the power saving mode a *constant* low level voltage is provided without variation, used for the same function that is less than 3.1V (Tsutsui, Fig. 3 element 300 and power save control signal). A person of ordinary skill in the art upon analyzing Tsutsui would have reasonably used any voltage values that are appropriate for different loads, including voltages less than 2.9V. The exact voltage values used are dependent on the voltage that is required to drive the load and are completely arbitrary, and therefore it would have been obvious to try voltages less

than 2.9V along with low power loads to achieve the predictable result of power conservation. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the power saving power supply of Tsutsui in place of the generic power supply of the AAPA in order to reduce power consumption.

Regarding **Claim 32**, the AAPA teaches a method for supplying a power to a liquid crystal display, having an interface circuit, a timing controller, a data driving circuit, and a gate driving circuit for processing digital signals (AAPA, Fig. 2), comprising the steps of:

providing a first power source voltage from a system wherein the first power source voltage is 3.3V (AAPA, Figs. 2 and 4 VCC);

supplying the first power source voltage of 3.3V to the interface circuit, the timing controller, the data driving circuit and the gate driving circuit for processing digital signal of the data driving circuit and the gate driving circuit (AAPA, Figs. 2 and 4 VCC elements 11-14);

generating a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH and a gate low voltage VGL from the first power source of 3.3V using a DC-DC converter (AAPA, Fig. 2 element 16); and

supplying the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 to the data driving circuit and supplying the gate high voltage VGH and a gate low voltage VGL to the gate driving circuit (AAPA, Fig. 2 element 14).

The AAPA fails to teach generating and supplying a second power source as claimed. Tsutsui teaches different power sources used for different parts of the display including the timing control circuitry and the driving circuitry, specifically:

generating a second power source voltage having a constant level of less than 3.1V from the first power source voltage of 3.3V using a reducing circuit (Tsutsui, Figs. 1 and 3 elements VDD1, VDD2 and VDD3);

supplying the second power source voltage less than 3.1V circuits other than the data and gate drivers (Tsutsui, Figs. 1 and 3 elements VDD1, timing controller).

With regard to the second power source voltage having a constant level of less than 2.9 V, a person of ordinary skill in the art upon analyzing Tsutsui would have reasonably used any voltage values that are appropriate for different loads, including voltages less than 2.9V. The exact voltage values used are dependent on the voltage that is required to drive the load and are completely arbitrary, and therefore it would have been obvious to try voltages less than 2.9V along with low power loads. Additionally, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the power saving power supply of Tsutsui in place of the generic power supply of the AAPA in order to reduce power consumption.

(10) Response to Argument

The applicant argues that the examiner has failed to establish that all four voltages are result-effective variables. However, since the applicant has failed to point out any criticality to the voltage of 2.9V, and no such criticality of that specific voltage is offered in the disclosure of the invention or applicant's remarks, the examiner does not

need establish that the four voltages are result effective variables. The voltages of 2.9V 3.0V and 3.1V have no significance to the application other than to be of different voltages. Tsutsui clearly teaches reducing a high voltage (5.0V) to a lower voltage (3.0V or lower) in order to save power. The examiner holds that reducing it even further down below 2.9V would be a trivial matter requiring no undue experimentation for one of ordinary skill in the art.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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Examiner, Art Unit 2629

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/Sumati Lefkowitz/
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